REMARKS

Claims 1 and 3-25 were remain pending in the application. Claims 1, 3, 5-8, 11-12, 15-16, 18-21, and 24-25 have been amended. Claim 26-29 have been added. Accordingly, Claims 1 and 3-29 are now pending in the application.

Support for claims 26-27 and 29 may be found, for example, on page 36 line 10 – page 38 line 27 and Figure 15 of the disclosure. Support for claim 28 may be found, for example, on page 38 lines 16-18, page 24 line 14 – page 26 line 11, and Figure 11.

Section 102(b) Rejections:

Claims 1 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bannon et al. (U.S. Patent Number 5,987,544).

Bannon teaches, at Column 4 Line 53 – Column 5 Line 11,

> "When one of the processors 13a, 13b, 13c, illustratively processor 13a, in the system 10 desires to determine the **status** of a particular block it (processor 13a) will execute a memory access on the bus 18. The interfaces 15b and 15c of the other processors 13b, 13c snoop on the bus and assert the shared signal and the dirty signal if the block corresponding to the address asserted in the memory access is dirty and if the block is present in their (processors 13b or 13c) respective caches. The processor 13a reads the other the processors 13b, 13c **duplicate tag stores 28b, 28c** to determine if the block desired by the requesting processor 13a is resident in the processors 13b, 13c backup cache."
>
> "If the block is present in the cache of 13b or 13c, the processor 13a also determines **from the duplicate tag store** whether **the dirty bit for that block has been set**. If the dirty bit has not been set then the processor 13a can go elsewhere such as main memory for the most up to date copy of the block. The system interface 15a then sends a set shared command to the processor 13b or 13c that had a copy of the block thus changing the state of the cache block to "shared"."
>
> "If the dirty bit has been set and thus the backup cache 26b or 26c contains the most current copy, the system interface asks the processor 13b or 13c to return

the block from the backup cache 26 or its other caches and then changes the state of the block to shared and dirty." (Emphasis added)

Additionally, Bannon teaches, in the Abstract,

> "A computer system includes a plurality of processor modules coupled to a system bus with each of said processor modules including a processor interfaced to the system bus. The processor module has a backup cache memory and tag store. An index bus is coupled between the processor and the backup cache and backup cache tag store with said bus carrying only an index portion of a memory address to said backup cache and said tag store. A duplicate tag store is coupled to an interface with the duplicate tag memory including means for storing duplicate tag addresses and duplicate tag valid, shared and dirty bits. The duplicate tag store and the separate index bus provide higher performance from the processor by minimizing external interrupts to the processor to check on cache status and also **allows other processors access to the processor's duplicate tag** while the processor is processing other transactions." (Emphasis added) (See also Column 3, lines 30-57)

Applicant respectfully submits that Bannon fails to teach or suggest, "a control logic operable to **read the dirty indicator and the corresponding redundant dirty indicator** from storage and to treat the block of memory associated therewith as dirtied if all or any one of **the dirty indicator and the corresponding redundant dirty indicator** has the predetermined state" as recited in claim 1. Applicant respectfully submits that Bannon teaches that to "determine the status of a particular block" the processor accesses only the duplicate tag store. In Bannon, the processor determines "whether the dirty bit for that block has been set" by accessing only the duplicate tag store. (Bannon, Column 4 Line 53 – Column 5 Line 11) Bannon fails to teach or suggest reading both "**the dirty indicator and the corresponding redundant dirty indicator**" to determine whether a block of memory has been dirtied. In fact, Bannon teaches away from the above-highlighted features of claim 1 by teaching, at column 3 lines 49-56, "This improves system performance since the processor bus and processor are not occupied with unnecessary tasks such as **informing other processor of the status** of its higher level caches" and at column 4 lines 44-47, "By providing a provision for storing dirty bits in the duplicate tag store, less interrupts are necessary to determine the complete **status of a block of data** in the BCACHE 24". Bannon also teaches, at column 2 line 66 – column 3

line 2, "the overall system protocol uses the DTAG [duplicate tag store 28] cache lookup **to determine the actual state** of a cache entry. As such, the DTAG status becomes the overall system's "**Point of Coherency**"." Applicant respectfully submits that the purpose of the duplicate tag store 28 is to eliminate accesses to the tag store 24a to check the status of a block of data. Therefore, in Bannon, since the processor only accesses the duplicate tag store 28 to determine state information, the processor may obtain inaccurate state information (e.g., whether a dirty bit corresponding to a block of memory is set) if the duplicate tag store has been corrupted.

In accordance, claim 1 is believed to patentably distinguish over Bannon.

Furthermore, independent claim 12 recites features similar to those highlighted above with respect to independent claim 1 and is therefore believed to patentably distinguish over Bannon for at least the reasons given in the above paragraphs discussing claim 1.

Section 103(a) Rejections:

Claims 3-10 and 13-14 were rejected under U.S.C. § 103(a) as being unpatentable over Bannon in view of Garnett (U.S. Patent Number 5,991,900). Claims 3-10 and claims 13-14 are dependent upon claim 1 and claim 12, respectively, and are believed to patentably distinguish over the Bannon and Garnett, whether alone or combined, for at least the reasons given in the above paragraphs discussing claim1 and claim 12.

In addition, Claims 15-23 were rejected under U.S.C. § 103(a) as being unpatentable over Garnett in view of Bannon, and Claim 24 was rejected under U.S.C. § 103(a) as being unpatentable over Garnett in view of Bannon and in further view of Watt.

Applicant respectfully submits that Garnett and Bannon, whether alone or combined, fail to teach or suggest, "each cycle including **reading a dirty indicator and a corresponding redundant indicator** from storage and treating a block of memory

associated with the dirty indicator and the corresponding redundant dirty indicator as dirtied if all or any one of **the dirty indicator and the corresponding redundant dirty indicator** has the predetermined state" as recited in claim 15. Applicant respectfully submits that Garnett and Bannon, whether alone or combined, fail to teach or suggest the above-highlighted features of claim 15 for similar reasons as outlined in the above paragraphs discussing Claim 1.

In accordance, claim 15 is believed to patentably distinguish over Garnett and Bannon, whether alone or combined. Claims 16-23 depend on independent claim 15 and are therefore believed to patentably distinguish over Garnett and Bannon, whether alone or combined, for at least the reasons given in the above paragraph discussing Claim 15. Claim 24 is also dependent upon claim 15, and is therefore believed to patentably distinguish over Garnett, Bannon, and Watt, whether alone or combined, for at least the reasons given in the above paragraph discussing Claim 15.

Additionally, Applicant respectfully submits that Garnett and Bannon, whether alone or combined, fail to teach or suggest, "wherein the storage comprises a lower level memory that includes groups of the dirty indicators **and groups of the corresponding redundant copies of the dirty indicators**, and at least one higher level memory that includes groups of dirty group indicators **and groups of corresponding redundant copies of the dirty group indicators**, wherein each dirty group indicator and a corresponding redundant dirty group indicator being settable to a given state indicative that a group of dirty indicators of the lower level memory has at least one dirty indicator in the predetermined state indicative that a block of memory associated therewith has been dirtied" as recited in claim 21. In accordance, claim 21 is believed to patentably distinguish over Garnett and Bannon, whether alone or combined.

Applicant respectfully submits that Garnett, Bannon, and Watt, whether alone or combined, fail to teach or suggest, "**reading a dirty group indicator and a corresponding redundant dirty group indicator** from the higher level memory and treating the group of dirty indicators associated therewith as dirtied **in response to all or**

any one of the dirty group indicator and the corresponding redundant dirty group indicator having the given state" as recited in claim 24. In accordance, claim 24 is believed to patentably distinguish over Garnett, Bannon, and Watt, whether alone or combined.

Also, Claim 11 was rejected under U.S.C. § 103(a) as being unpatentable over Bannon in view of Watt (U.S. Patent Number 6,272,033). Claim 11 is dependent upon claim 1, and is therefore believed to patentably distinguish over Bannon and Watt, whether alone or combined, for at least the reasons given in the above paragraphs discussing claim 1.

Additionally, Applicant respectfully submits that Bannon and Watt, whether alone or combined, fail to teach or suggest, "wherein the storage comprises a lower level memory that includes groups of the dirty indicators **and groups of the corresponding redundant copies of the dirty indicators**, and at least one higher level memory that includes groups of dirty group indicators **and groups of corresponding redundant copies of the dirty group indicators**, wherein each dirty group indicator and a corresponding redundant dirty group indicator being settable to a given state indicative that a group of dirty indicators of the lower level memory has at least one dirty indicator in the predetermined state indicative that a block of memory associated therewith has been dirtied" as recited in claim 11. In accordance, claim 11 is believed to patentably distinguish over Bannon and Watt, whether alone or combined.

Furthermore, Claim 25 was rejected under U.S.C. § 103(a) as being unpatentable over Bannon in view of Gilham (U.S. Patent Number 5,987,544). Claim 25 is dependent upon claim 1, and is therefore believed to patentably distinguish over Bannon and Gilham, whether alone or combined, for at least the reasons given in the above paragraphs discussing claim 1.

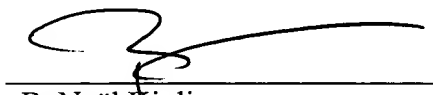
Also, Applicant respectfully requests examination of added Claims 26-29, which are believed to patentably distinguish over the cited references, whether alone or combined.

CONCLUSION

In light of the foregoing amendments and remarks, Applicants submit that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-03100/BNK.

Respectfully submitted,



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